

FILENAME: PBUFF_K.TXT

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Don McKENZIE
29 Ellesmere Cres.,
Tullamarine 3043
Australia
Phone (03) 338 6286

PRINTER BUFFER ASSEMBLY INSTRUCTIONS
SIZES RANGE FROM 8K TO 4Mb.

ASSEMBLY INSTRUCTIONS FOR THE REVISION "K" PBUFF SHORT FORM KIT.
Covers Versions 3.2/2.2 and Version 5.1E (8K to 4Mb)

QUICK INSTRUCTIONS FOR VERSION TYPE CONFIGURATION:-

AN EPROM MARKED "PK" IS VERSION 5.1E (64K to 4Mb) The J6 jumper must be linked to the "L" pad. All 8 DRAMS (or single module, see below) must be installed. These DRAMS can be 4164's, 41256's, or 4C1024's, or 4Mb. Memory jumpers M1 to M7 must be configured for the correct DRAM type as shown on the dual "before and after" type overlay. The DRAMS must also be inserted into the correct position in the 20 pin sockets. This information is also shown in the dual overlay. The 8K static ram (E14) and the 555 timer (E15) must be installed for the buffer to operate.

AN EPROM MARKED "PC" IS VERSION 3.2/2.2 (8K to 256K). To select V3.2 (256K), link the centre pad of J6 to the "L" pad. The full 256K must be installed. To select V2.2, link the centre pad to the "H" pad. This will select the high bank of the EPROM which is V2.2 This version uses 4164 type DRAMS and can be configured for either 8K, 16K, 32K or 64K. The 8K static ram (E14) is not required for the "PC" version, and the 555 timer (E15) must not be installed. If the 555 timer is installed, the buffer will not operate.

ALTERNATIVE MEMORY MODULE INSTALLATION. Version 5.1E Only...

If a 30 pin (Any size up to 4Mb) MEMORY MODULE is to be installed, then YOU MUST SET the M1 to M7 blocks to the 64K/256K settings.

The 8 by 20 pin sockets mentioned in the following instructions are not needed. The bypass caps. BC1 to BC8 are also not required. Both SIPP and SIMM types can be installed. One has pins, the other has pads. The lead variety may be soldered into the board, the lead-less can have a strip of male pins soldered to it which in turn can solder into the board. The hole sizes in the board are large enough to accommodate a standard strip of 30 male pins, or wire-wrap size pins.

You may wish to use the snap away type machine sockets to manufacture a 30 pin single row socket and solder it into the board so that it will accommodate your lead type module. The module socket is marked on the component side of the board, as is pin 1. This means that when installed, the DRAMS will face away from the board. 8 or 9 byte wide modules can be used. PBUFF ignores the ninth byte.

20-JUN-92 ROD IRVING ELECTRONICS has SIMM Sockets available. P10536 \$5.95 is a single row, and P10538 \$6.95 is double row. You should be able to easily split the double row into a single if needed.

Four early warnings:

(1) The I.C.'s on my boards are tightly packed. Make sure that your sockets fit into the board before soldering them in. Chunky sockets will not match up with the .1 inch centres between chips.

(2) The PBUFF board is easily ruined by soldering the components onto the board the wrong way. The component side is marked. The header pins, capacitors and resistors mount on the component side. The DB25F will only mate with the edge connector one way, that is with the widest part of the connector down. The CENT36F mounts the same way, widest edge of the connector down when looking at the component side of the board. Be warned!! . Some kit builders still get it wrong.

(3) When drilling those holes in the front of your case, make sure that the front panel hardware doesn't interfere with the components on your PBUFF board.

(4) If you run PBUFF at 6Mhz or greater, you may need a 330 Ohm pull-up resistor on the CPU clock line. This is mentioned in these instructions when I cover CPU speeds and just before we dive into the main assembly. So I mention it again. In fact, I now recommend that this resistor be installed for all clocks over 4Mhz. The best place to install this is on the solder side of the board at E10, the CPU 40 pin socket. It connects between pin 6 (clock) and pin 11 (+5V).

ARTWORK FAULT *****

THIS FIRST REVISION K BOARD HAS AN ARTWORK FAULT THAT CONNECTS GROUND AND +5 VOLTS TOGETHER. THIS SHORT IS ON THE COMPONENT SIDE OF THE BOARD AT THE LEFT HAND HOLE OF BC5 (ABOVE E5). I HAVE CUT THIS TRACK FOR YOU, BUT JUST IN CASE I MISSED YOUR BOARD, CHECK FOR A SHORT BETWEEN GROUND AND +5VOLTS WITH A METER.

Items supplied in kit:- One bare double sided, plated through printed circuit board, one EPROM programmed with the ordered version of PBUFF, and these assembly instructions.

All text is supplied on a 3.5" 720K IBM format floppy disk. Files included are a rom image of the current Version PBUFF as well as the alternative Ver3.2/2.2.

PBUFFTST, a printer buffer test program will also be found on this disk. This is a compiled TurboBasic program. Source code is included for this program.

Photocopies of all Circuit diagrams, and Overlays are included.

The kit builder should have a reasonable tool kit which will include a Multi-Meter. A logic probe may be needed to help you with any hardware problems that you could run into. The logic probe I use is a 3800A. It is available at most electronic outlets for around \$35.00 Don't rush out and

buy a logic probe because I said you may need one, you probably won't, but if you do run into real strife then it may be the only way out.

Single and/or Dual strips of male header pins can be used for memory configuration points, and other header positions if you wish. Test links can be used to alter these link settings easily.

The following items are needed to complete the project:- I have broken this into Section A, Section B, and Section C. Section A items are needed only if you don't have an existing power supply capable of delivering +5 volts at around 300mA. I have used Dick Smith Catalogue numbers on some components only for reference purposes. You may find other outlets more convenient.

SECTION A. (External power components.)

Plug-pack 9 volts AC or DC at 400-600mA. The current required to run the full 8 memory chips is just under 300mA, but I would recommend a larger supply than this as a safety margin. PBUFF will accept AC or DC input. Experienced builders may prefer to use a suitable AC transformer. (DSE Cat M-2155 9.5VAC multi-tap @ 1A)

IF YOU WISH TO ADD A SERIAL BOARD LATER ON, THEN A 9 VOLT AC SUPPLY MUST BE USED SO THAT -12 VOLTS CAN BE GENERATED FOR IT'S RS232 CIRCUITS.

Diode Bridge D1 WO2 or WO4 type. (DSE Cat Z-3304)

Capacitor C3 10uf Tantalum @16 Volts.

Capacitor C4 2500uf Electrolytic @16 Volts. (PCB type mount.)

7805 +5 Volt regulator in TO-220 case.

A "U" shape type heat sink to suit regulator.

Section B. (Main board components.)

Capacitors	BC1-BC11	.01uf Ceramic (11) (bypass)	Resistor	R1	100K
Capacitor	C1	220pf Ceramic	Resistor	R2	270 OHMS
Capacitor	C2	22uf Tantalum @16 Volts.	Resistor	R3	10K
Capacitor	C5	150pf Ceramic ** NOTE	Resistor	R4	330 OHMS
Capacitor	C6	680pf Ceramic	Resistor	R5	1K
Capacitor	C7	.01uf Ceramic (V5.1E only)	Resistor	R6	4K7
Capacitor	C8	.01uf Ceramic (V5.1E only)	Resistor	R7	100K (V5.1 only)
			Resistor	R8	1K (V5.1 only)
			Resistor	R9	220 OHMS
			Resistor	R10	4K7
			Resistor	R11	270 OHMS

Resistor Network SIP package, 7 x 4K7 resistors with one common pin. (8 pin device)

Optional Resistor Network SIP package, 9 x 4K7 resistors with one common pin. (10 pin device) for V5.1E only. READ TEXT.

Z80A (Z80B) CPU 555 Timer I.C. (V5.1E only)

8255 Programmable Peripheral Interface 6264 8K by 8 SRAM (V5.1E only)
74LS00 Quad 2-input nand gate.
74LS04 Hex inverter.
Crystal 3.58 Mhz in a small case. (DSE Cat K-6031)
 (Z80B can use up to a 6.17 Mhz crystal.)

Transistor Q1 BC548 Any NPN Small Signal Amp will do.
 (BC108, BC148, BC208, or DSE CAT Z-1308 DS548)

VERSION 2.2 ONLY.... 4164(s) 64K dynamic rams. One required for 8K, two for 16K, four for 32K, and eight for 64K. Any type are suitable, as the software provides for both 7 bit and 8 bit address refresh. This includes Texas Instruments TMS 4164's.

VERSION 3.2 ONLY.... 41256's 256K dynamic rams. Eight required.
(or 256K MEMORY MODULE>

VERSION 5.1E ONLY.... Full eight dynamic rams. Uses 4164's, 41256's, or 4C1024's. (or 64K/256K/1Mb/4Mb MEMORY MODULE)

Section C. (Misc. components.) Chip sockets:- My usual rule is to fit sockets to all 40 pin devices, all ROM, and all RAM. This only leaves the two 74 series chips and the 555 timer without sockets, so my advice is to fit sockets for all I.C.'s. If you experience problems debugging the hardware of this project then sockets will be a life saver. Sockets required:-

40 pin (2)
28 pin (2)
20 pin (8) 64K (4) 32K (2) 16K (1) 8K
14 pin (2)
8 pin (1)

If you wish to expand your memory at a later stage, then it would be advisable to fit the full eight RAM sockets now.

Version 3.2 and later..... The full 8 sockets must be fitted.

Two push button (make) momentary switches for the RESET and TEST buttons. SPST switch for the COPY switch. (Optional hardware pause SPST switch.) Two red LED's 5mm, and LED mounting bezels. (DSE Cat Z-4030, and H-1910) A suitable case. I have designed the board mountings to fit the Dick Smith Cat H-2505. This is a superb plastic instrument case at a low cost.

CENTRONIC CONNECTORS ASSEMBLY..... This is the last thing you do.

I have mentioned this first because you must do it last. Why? It's the part you can muck up very easily, and turn your board into scrap. So I get you to read it first.

This can be done in one of two ways. Read through both options fully before making a final selection on the option you wish to choose.

OPTION [1]

A standard DB25 solder tail connector is soldered onto the edge of the board into the position shown on the overlay. The female Centronics solder tail connector (or chassis type mount) will not be hard to obtain, but there are several types around. Some have spring clips that lock onto the male connector. The clips are nice, but as I have found, the standard (non-clip) connectors do lock hard onto the male connector quite firmly.

The point to watch out for with the Centronics female connector is the distance between the two rows of solder tails. Lets say that a standard printed circuit board is about as thick as a 10 cent piece. (That's OZ money digger!!), which as a rough guide, it's close enough. Well, if you can slip a 10 cent plus a 20 cent piece, or two 20 cent pieces between the rows of pins, then you will have a lot of trouble trying to solder this type of connector to the edge of the board. Look for a connector that has the two rows close enough together to be able to solder to the edge of a printed circuit board. You may find a connector that has the wide rows of pins, but the pins are very easy to bend. Even with your finger. These type can be readily crimped in a vice to align the pins closer together.

The pin numbers of the two connectors are marked on the PBUFF board.

You will need to use a file to bevel a slight 45 degree angle along the DB-25 connector tracks so that the DB-25 connector will push hard onto the board without damage. Looking at the overlay side of the board, the two female connectors should have the widest part facing down. They can be soldered into position when the rest of the board has been assembled.

The board can be mounted to the rear of your case using the two outer mounting holes of the DB25 and Centronics connectors only if you wish.

Your existing cable plugs into the female Centronics. (INPUT) A standard IBM PC type cable plugs into the DB-25 female connector. (OUTPUT)

OPTION [2]

I have allowed provision for standard 26 wire (25 wires only used) IBM type I/O connections at J8 and J9 which may suit kit builders that wish to install PBUFF inline using flat ribbon cable. This also allows easy installation inside computer cases.

If you wish to, you can crimp 26(25) wire flat ribbon cable to IDC headers for the J8 and J9 wiring, and run them out to externally crimped DB25 connectors at the rear of your case. This also means smaller holes are required to get the wiring out of your case. It gives you a lot of options.

Some IBM users that had PBUFF running for some time now, (like about 1985) found that "NEW" software was checking the error line and PBUFF was bombing out. The circuit takes care of all of the handshake problems known to date. This forces the computer to handshake to the buffer, and the buffer to handshake to the printer.

Don't let the IBM type cable scare you, This board simply converts from your

existing Centronics input cable to IBM standard. The IBM cable then converts back to standard Centronics, and it's cheap.

NOTE **** Don't install any DRAM Memory until you have been told to do so. Read the instructions. Version 5.1E allows printer testing of the buffer before committing your expensive DRAMs to the project.

Before we dive into the assembly, a word on CPU speeds and problems.

The circuit as is, will run a Z80A with a crystal frequency up to 4Mhz. In most cases, it will run a Z80B with a crystal frequency of 6.17Mhz.

If it doesn't, install a 330 Ohm resistor between E13 pin 14 and E13 pin 4. This will pull the clock to a higher voltage than the normal TTL level, which is ideal for the Z80 clock. Zilog recommend this value resistor as a pull-up. This circuit will usually run a Z80B at up to 8Mhz. Certainly, it will make the clock circuit more reliable for 6Mhz operation.

By installing a 1K resistor between E13 pin 7 and E13 pin 6, a 10Mhz crystal may be usable with either a Z80B or a Z80H. This is the output strobe signal to the printer.

If you are experimenting with faster speeds, it may pay you to fit the 10 pin resistor network mentioned later. This is fitted to the solder side of the board onto the 8255 socket, and pulls the data bus to a known level.

The Z80H is rated by Zilog at 8Mhz. Some people refer to this 8Mhz device as a Z80C, but I have yet to see a data sheet on a Z80C.

Zilog chip numbers now look like this:

Z0840004 is a Z80A, Z0840006 is a Z80B, and Z0840008 is a Z80H.

2-Jun-92 Speed Notes...

I have been able to run a Z80B and a Z80H at 10.6445Mhz. Both failed to run at 12Mhz, and so they should!!!

The Z80H required C5 (150pf) to be installed when no Front Panel was used.

Below is a screen dump of PBUFFTST results when the 10.6445Mhz crystal was used on a 4Mb PBUFF driven with a 386SX 20Mhz system:

C:\>PBUFFTST 64

64 Page(s) selected. 4096 K

Written	Percentage
4095 K	PBUFF full or reset pressed.

Bytes written	Bytes installed	Bytes rejected
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4,194,240

4,194,304

64

Rejected bytes should equal number of pages installed in PBUFF

These calculations have taken into account one byte that is latched into the 8255 but has not yet been written to Drums.

Time elapsed = 267.16 seconds. Average load rate = 15699 bytes per second.

This is approximately 942 K bytes per minute.

C:\>

The above results are about the same when a 12Mhz 286 system is used.

PBUFFTST wouldn't work on the 386SX when a 3.58Mhz crystal was used. It always sensed the buffer as being busy or not connected. I needed to beef the frequency up to a 6Mhz before getting results. No doubt the 386 is too fast for this test. PBUFF still operated correctly as a printer buffer under these conditions...

THE REAL ASSEMBLY:- Can't think of anything else that we need, so if you have all of the above parts let's get to it. With your multi-meter check that ground and +5 volts are not shorted together. As you progress along, do the same test for +5V and ground shorts at regular intervals, as these two signals go to every chip, and at least one signal to almost every other component, they are the most likely to short due to soldering faults. They are also the hardest fault to find and isolate when all your sockets are installed.

Have a look at the Printer Buffer Overlay. This is drawn from the component side of the board. Now look at your printed circuit board. The component side is marked. The other side is the solder side. This is marked with the words "SOLDER SIDE".

Examine the board on both sides for defects before assembly. Any fault on the solder side can be easily fixed, but once you have your sockets in, the component side of the board is impossible to fix without removing these sockets, so pay particular attention to the component side artwork before assembly. Check any suspicious sections with a meter.

Install the I.C. sockets into the board. Take note of the orientation of pin 1 of the I.C.'s, as I have not arranged the direction of the chips in a logical fashion. This has been done to minimize the size of the board.

Pay particular attention to the 8255 pin 1 position. This is in the opposite direction to the other I.C.'s.

NOTE *** Rev K board has three extra positions for user prototype IC's. Ex and Ey are 16 pin, and Ez is a 20 pin device. Ground and +5V have been connected to the appropriate pins. Sockets do not need to be fitted to these

3 positions. They are only for experimental or custom hardware.

VERSION 2.2 (8K-64K) SOCKETS AND BYPASS CAPS.....

The RAM software drivers require the most significant bytes to be installed first, that is, an 8K buffer needs only the data bit 7 RAM chip installed. This is shown as E8 on the overlay. Capacitor BC8 is the bypass capacitor for E8. Best I give you a table at this stage for the various memory sizes.

RAM chip configuration:-

	4164(s)	Capacitor(s)	
8K	install E8	and BC8	(Data bit 7)
16K	install E8,E7	and BC8,BC7	(Data bits 7 and 6)
32K	install E8,E7,E6,E5	and BC8,BC7,BC6,BC5	(Data bits 7,6,5 and 4)
64K	install all RAM chips	and all bypass capacitors.	

Version 3.2 and 5.1E ...

Install all RAM chips and all bypass capacitors. Once you have determined which sockets are to be installed and have them in position, they can be soldered in.

Install the 8 pin resistor network into the board as shown on the overlay, that is with pin one towards the dynamic rams, and solder in.

Install all the resistors as shown on the overlay into their mounting holes. They can now be soldered in and the legs cut off flush with the solder joint.

Install the BC capacitors. (Refer to RAM chip configuration.) Install C1, C5, C6, C7, and C8 capacitors. Solder these caps in and trim off the legs as before.

NOTE *** C5

Try to get the circuit running before installing C5. If it runs without C5 installed, this will save you the trouble of removing it later if you are installing a Front Panel I/O board. C5 is used to trim the chip select to write timing of the Z80/8255 combination. In most cases, the circuit will work without C5. My early versions of single sided boards always needed C5 installed before they would work.

HEY !!!! Instead of me saying solder in component "X" and trim off the legs, you just add "AND TRIM OFF THE LEGS", every time I mention "SOLDER IN", OK?

Capacitors C2, C3, and C4 are polarized and must be soldered in the correct way around. These caps. have a plus sign (+) on one end of them, or in the case of C4, a minus sign (-) on one end. Solder them into the board as per the overlay.

Install diode bridge D1. Take notice of the markings on the bridge and make sure that these line up with the overlay.

Solder in the 7805 regulator. The words "7805" must be facing towards the

diode bridge. Fit the heat sink to the 7805.

Position transistor Q1 into the board. If you use a DS548, the "CBE" connections are marked on the case and line up with the overlay as far as the flat side is concerned. The BC548 and the others, although not marked, should mount into the board the same way. If you end up with some obscure brand that you are not sure of the pinout, try reversing the Q1 connections if the clock fails to run.

Solder in the crystal, don't push it fully into the board, but leave enough length on the legs so that it will not short out the tracks underneath.

FRONT PANEL CONTROLS.....

J3 (Control) has been set out in a 16 pin dual row header. If you wish to, a 16 pin header, crimp connector, and approx. 9 inches of 16 wire flat ribbon cable may be used for front panel wiring. Don't cut off the spare wires. This wiring can also be done without the headers etc. as follows:-

RESET button..... Connect two insulated wires (approx. 9 inches long) from the reset button to the two points as shown on the overlay.

COPY switch... The same wiring method as the reset button, a pair of wires connected from the holes marked COPY to the SPST switch.

TEST BUTTON..... Same method as RESET button.

DATA LED..... The LED has one leg longer than the other. The longest leg is the anode, and the short leg is the cathode. Connect an insulated wire from the anode to the hole marked LED+, and from the cathode to the hole marked LED-. (See overlay.) The cathode leg can also be found by the "FLAT" edge on the LED itself.

OPTIONAL POWER LED.... Same method as the DATA LED.

OPTIONAL HARDWARE PAUSE.... Same as above again, but connected to the two "pause pads". Two additional square pads on the component side of the board between J3 and Ez are the isolated pause pads. These may be joined at this point if you don't require the Pause feature.

All floating wiring goes into the component side of the board the same as any component.

J1 HEADER.....

FUTURE EXPANSION, NOT USED FOR Ver 3.2/2.2, however V5.1E uses it for my FRONT PANEL I/O BOARD, and C3P1 BOARD. A 40 pin header can be soldered into this position to extend the Z80 bus pinout. Pin 1 of J1 is also pin 1 of the Z80, pin 2 is pin 2 etc. This is fully detailed in the circuit.

J2 and J7 HEADERS.....

These headers can be ignored unless you require to fit additional boards such as Serial, and switch boards. Do not cut the tracks between "A" & "A" unless you are fitting additional boards.

If required, Two 26 pin male headers can be soldered into the J2 and J7

positions. Using 26 pin IDC type crimp headers and flat ribbon cable, connections can be made to other I/O boards or connectors. Tracks that are connected between "A" and "A" on the component side of the board will need to be cut for additional boards.

J4 SERIAL BOARD POWER OUT.....

Used only for the SERIAL board. The AC connection is used to generate -12V on the SERIAL board. A strip of 2 male pins must be soldered into these pads if a serial board is to be used.

J5 8255 Chip select....

The stand alone PBUFF board must have pad X connected to pad Y for normal operation and is Reconfigured when a Front Panel I/O board is installed. The FPIO board has a port decoder chip on board and the 8255 chip select must be isolated from the IORQ signal and jumpered to the PORT 0 signal. For Front panel operation, pad Y must connect to pad Z. Capacitor C5 must also be removed for Front Panel Operation.

The pads marked GND & +5 are used for test connections. Two posts can be soldered into these pads.

Don't install the chips yet. Connect up your power-pack, transformer, or +5 volt supply. The power pack connection points are shown on the overlay. As the circuit has a diode bridge at the input, it doesn't matter which way around you connect the positive and negative terminals. If you are using an existing +5 volt supply then connect the power up to the +5volts and ground "POSTS".

With your multi-meter check that ground and +5 volts are not shorted together. Power up the unit and check that the +5 volts is there before proceeding. Check the polarity of the +5 volts. All OK? Power down and install chips E12 (8255) and E13 (74LS04).

DON'T---DON'T---DON'T---PUT ANY CHIPS IN THE WRONG WAY AROUND. YOU WILL MOST CERTAINLY DESTROY THEM!!!!!!!!!!!!!!!!!! CHECK THE OVERLAY FOR PIN 1 ORIENTATION. THE NOTCH UP ONE END OF THE CHIP, AND THE SMALL BLACK DOT SHOWS PIN 1 LOCATION. YOU WILL FIND SIMILAR MARKINGS ON EACH CHIP. Power up again and check the +5 volts. If the LED is not already on, press the reset button. The LED should light up brightly.

NO LED?.....

Then you have one of the following faulty:- E12, E13 ,RESET button, reset circuit, LED, LED circuit, or more likely you have the LED wired in back to front. LED OK?..... Power down, and install E9 (74LS00), E10 (Z80A/B), and E11 (EPROM), and power up.

NOTE ***** VERSION 5.1E AND LATER.....

Additional kit builder diagnostic information and operating instructions differ from earlier Versions as the static ram and 555 interrupt tests have been added. This section follows the Version 2.2 and 3.2 instructions.

Version 2.2 and 3.2 diagnostic instructions:-

The LED should be flashing at approx. 1 cycle per second. If the LED is flashing, it indicates that the Z80 is running and the software is doing it's job, but a RAM fault exists. With no RAM installed this is to be expected. If the LED doesn't flash then move on to the "IT DOESN'T WORK DEPARTMENT".

Happy and no smoke? Good it's time to insert one RAM chip. Power down and insert a RAM chip into socket E8 (Data bit 7) watching out for pin 1 (look at the overlay.) COPY ON/OFF..... The copy switch is in the COPY ON position when the switch contacts are made, and in the COPY OFF position when the switch contacts are open. Switch to COPY ON, power up and check your volts again.

At this stage, the LED should be flashing at approx. 3 cycles per second, which indicates that RAM is present and can be written to and read from.

Switch to COPY OFF. The LED should go out. Press the reset button. The data LED should light up brightly. Release the reset button and the LED should go out. This indicates that the software is working.

All looking OK? Power down, install additional RAM chips to suit your memory requirements, (Version 3.2 all eight 41256's must be installed.) and power up again. Repeat the above simple test procedures using the COPY and RESET switches. A simple RAM test is performed before the LED will flash.

This test may not show up a shorted track, or a faulty RAM in some cases. If you have a suspect RAM, it can be further tested on it's own in the DATA bit 7 position by setting COPY ON, power up, and the LED should flash at approx. 3 CPS. If at any time the LED flashes at approx. 1 CPS. then a RAM fault has been detected.

LOOPBACK TEST ...

What still happy? Power down, connect the output port pins 1 (STROBE), 10 (ACK), and 11 (BUSY) to the input port pins 1, 10, and 11. This can be done by simply plugging the input and output of your IBM printer cable into the BPIO board. If your input and output can't readily be connected together, then 3 jumper leads can be used to connect pin 1 to pin 1 etc. When this has been done, set COPY OFF, power up, and press TEST.

The TEST function outputs a sign on message to the printer. In this case, it outputs a string of characters to it's own input port that keeps cycling through the buffer until RESET is pressed. The TEST function will light up the DATA LED to about half brilliance.

Still happy? Power down, connect a printer, set COPY OFF and power up and press TEST. If all is well you should get the sign on message complete with memory size information. When the test facility is used, a ROM check is also done. If any byte in the ROM is incorrect then an error will be reported on the printout.

Power down, have a quick read through the OPERATOR INSTRUCTIONS, connect your computer to the input plug. Power up, and try printing a file. It

either works OK, or doesn't work at all. If it works then you can slap it in a box, and forget it. Bob's your Uncle. If it doesn't work then go on to the "IT DOESN'T WORK DEPARTMENT".

End of Version 2.2 and 3.2 diagnostic instructions.

ADDITIONAL ASSEMBLY INSTRUCTIONS AND DIAGNOSTIC TESTS FOR VERSIONS 5.1E AND LATER.

INSTALL 8255 AND 74LS04.... Power down and install chips E12 (8255) and E13 (74LS04). Power up again and check the +5 volts. If the LED is not already on, press the reset button. The LED should light up brightly. LED OK?.....

INSTALL 74LS00, Z80, AND EPROM... Power down, and install E9 (74LS00), E10 (Z80), and E11 (EPROM), and power up. The LED should be flashing at approx. 4 cycles per second. If the LED is flashing, it indicates that the Z80 is running and the software is doing it's job, but a STATIC RAM fault exists. With no STATIC RAM installed this is to be expected. If the LED doesn't flash as expected at any time during the construction of this kit then refer to the "IT DOESN'T WORK DEPARTMENT" in the main instructions.

INSTALL 6264... Power down, install E14 (6264) and power up. LED should be on most of the time and flash to off for a short period. This indicates a pass of the 6264 and a fail of the 555 timer. Well, once again expected if the 555 IC isn't installed.

INSTALL 555..... Power down, install E15 (555), and power up. The 555 timer is used to interrupt the Z80 so that controlled refresh of dynamic rams can be achieved. For the technically minded, the output of the 555 timer pin 3 has a duty cycle of 7.5us low and 750us high. During power up or reset, the LED lights up for one flash then goes off. Another four flashes are then produced. This new flash rate is about two cycles per second. The combination of the first flash followed by another four appears to look like five flashes.

LOOPBACK TEST... During the above test, when the LED finally stops flashing, the buffer is attempting to output it's TEST MESSAGE. Connect the input and output of the buffer together. If you have used my BPIO board, then a standard IBM type cable can be used for this connection. If your input and output can't readily be connected together, then 3 jumper leads can be used to connect the output port pins 1 (STROBE), 10 (ACK), and 11 (BUSY) to the input port pins 1, 10, and 11. If the loopback test is successful, the LED will flash four times, the test message is written to the output cable which is also the input cable, the LED again flashes four times, the test message is written, and on it goes until you either break the loopback connection, set hardware pause on, (if fitted) or power down. The test message is not seen readily as activity when looking at the DATA LED, so this test almost appears to be a continuous flash of around two cycles per second.

NOTE *** If the hardware pause switch isn't fitted, the pause pads must be shorted to enable the loopback test, and in fact to enable the buffer.

PRINTER TEST... Conditions still as above. You should have no Dynamic Rams installed yet. Connect the buffer output to a printer. The DATA LED will flash four times, the TEST message will be printed, LED flashes four times, print test, four flashes, etc. Very informative the test message. It not only tells you the name of the bloke to blame for getting you into this mess, it also tells you if you have a "ROM CHECKSUM ERROR". If no error is reported then the EPROM looks in good shape. It also goes on about possible faulty Dynamic Rams. Need I say it again. Yes, not yet installed. See below.

INSTALL DYNAMIC RAMS... Before installing Drams, a little story. No Drams in sockets, nothing but a big hole. When the Z80 tries to read from these holes, the data bus is in an unknown state. Might think that any individual data bit is a high, or it might think that its a low. It's not really a problem. If you have a DRAM, DRAM socket, or Dram bus (usually a solder joint) fault, then the hole becomes a problem. The Possible Faulty RAM test tends to be a bit of a fairy story until you set the data bus into a known state. More on this later.

The software detects the difference between 4164's, 41256's, 1Mb, and 4Mb chips, so power down, and install your first dram (or full Memory Module in its appropriate position) into any socket E1 to E8, and power up. The test message will tell you if this data bit (DRAM) is good simply by not showing it as faulty, but this may not be true because of the floating data bus during the dynamic ram test. Ambiguous? Yes, I thought so too, and I wrote it. The idea is to install the drams one at a time as explained above, and watch the floating bad data bits test printout reduce as you increase the chip count. When all eight chips are successfully installed, a new set of rules apply. See DRAMS INSTALLED SUCCESSFULLY section below....

DRAM FAULT STILL... If you get stuck at this point, then you will need to set the data bus into a known state to be able to seek out any dram associated fault. And it's simple. Install the above mentioned RN10-4K7 resistor network as follows:-

On the solder side of the board, position the resistor network neatly under the 8255 PPI so that pin 1 of the resistor network lines up with pin 26 (+5V) of the 8255 and the last pin of the resistor network lines up with pin 35 of the 8255. Each of the ten pins can be soldered to the socket pins. Make sure that the resistor network is laying flat on the PC board under the 8255 position. The TEST printout will now indicate a true DRAM, socket, or solder fault. For example, if D0 is faulty, then the fault is at the E1 position. You could try swapping the DRAMS to prove the D0 chip. More likely, it will be a soldering fault. In a small percentage of cases it could be a socket fault.

DRAMS INSTALLED SUCCESSFULLY... Switch to COPY ON and power up. At this stage, the LED should be flashing at approx. 4 cycles per second, which indicates a pass of all system diagnostics. Switch to COPY OFF. The LED should go out. Press the reset button. The data LED should light up brightly. Release the reset button and the LED should go out.

Power down, connect your printer, set COPY OFF and power up and press TEST. If all is well you should get the sign on message.

Power down, have a quick read through the OPERATOR INSTRUCTIONS, connect your computer to the input plug. Power up, and try printing a file. It either works OK, nearly, or not at all. If it works then you can slap it in a box, and forget it. Bob's your Uncle. If you seem to be almost getting a correct printout but some characters are repeated or incorrect, try printing an "ABCDEFGH" etc., alphabet type file. This often points you towards a data bit fault.

If the test message is correct, then the internal data bus between EPROM, Z80, and the 8255 has been proven. Also the 8255 external output printer signals. The TEST message will tell you about your DRAMS. The only area not proven at this stage is the input signals to the 8255. If one of these is missing then incorrect data will be written to the DRAMS. If it doesn't work then read on to the "IT DOESN'T WORK DEPARTMENT".

End of Version 5.1E diagnostic instructions.

"IT DOESN'T WORK DEPARTMENT."

ARE THE PAUSE PADS SHORTED OUT ON J3? They should be if no switch is fitted. WITH A FAST CRYSTAL (6Mhz and up), 330OHM PULLUP INSTALLED?

YES, with the full RAM installed, the 7805 will get warm enough to burn your finger, but no other component should. I don't intend to hand feed you a step by step "POWER UP, POWER DOWN, POWER UP" type format. Any time you plug or unplug any connector or chip then all power must be turned off. Disconnect the input and output plugs. Let me outline the five major faults found in kits:-

- (1) Bad socket solder joints. (open circuit)
- (2) Faulty socket connections. (open circuit)
- (3) Solder shorts between tracks. (short circuit)
- (4) Point not soldered. (open circuit)
- (5) Artwork or tracks faulty. (open or short.)

Faults 1 and 2 can usually be found with a logic probe. Any pin on any chip should be in one of three states. High, low, or bobbing. Well almost every pin. If no LED's light up, this is known as a high impedance state. Check over all chips for ground, +5 volts and other signals. Make sure that there are no high impedance states anywhere.

Exceptions to the rules:- The input and output ports of the 8255 could show anything random as this may not get programmed correctly on power up. The data bus may also show high impedance states under certain conditions. Pressing the reset button will bring some life into the data bus. If a high impedance state is found where it shouldn't belong, then check with your meter for a connection between the solder pad under the board and the pin of the chip for zero ohms. If you find no connection then pull out the chip and check between the solder pad and the socket connector itself.

Still no connection? Try soldering this point again. If this doesn't work then you could be up for a complete socket replacement. A nasty job for a newcomer. Sometimes, bending the legs of the chips at a slightly different angle, or just pulling and re-inserting a chip can remove socket problems.

Faults 3 and 4 are ones that you have created. A close visual inspection and perhaps a check around with an ohm meter will usually overcome this fault. A magnifying glass may help you.

Fault 5 is the result of my board manufacturer. Should never happen, but it does from time to time. I have threatened him with instant death if it happens again. Can be overcome using faults 3 and 4 detecting methods.

CLOCK SIGNAL CHECKS.....

With a logic probe check E10/6. This should be bobbing up and down, as this is the clock signal. No clock? Remove E10 and check E13/4 for activity. Still no clock? Check E13/3. If no clock is found here, try removing E13 and test the socket contact of E13/3. No clock? It has to be one of the following:- Crystal, C1, C6, R1, R2, or Q1. Is Q1 connected the right way around?

If you are getting the clock to pin 6 of the CPU socket without the Z80 in, and no clock with the Z80 in, then it may be the Z80 itself.

If you have a good range of spare chips then substitution may bring results.

CLOCK WORKING, BUT STILL NO RESULTS?

Remove E7 and check that the LED flashes at approx. 1 CPS. The software checks the RAM and if none is present the LED is flashed at the slow rate. If this checks out OK, then it should mean that the system is working up to the point short of a RAM check. Install E7, set COPY ON and check for the faster flash rate. If this checks out then it appears that the system is working.

OK, where do we go from here?

When the input and output plugs are connected together, COPY OFF, and TEST pressed, pins 1,10, and 11 should be bobbing. Press the reset and check the MREQ line, Z80 pin 19. If it is bobbing then the CPU is attempting to read the ROM. Press the reset and check the IORQ line, Z80 pin 20. If this is active then the CPU is attempting to access the 8255 ports. Check all ROM and RAM signals. All pins except ground and +5 volts should be active.

The CPU.... Activity on most pins. Reset can be checked using the reset button. Pin 26 should be low when the reset button is pressed and high when the reset button is released. E13/8 should show the inverse levels to the CPU/26. (See the reset circuit diagram.) The 8255/35 should be the same levels as E13/8. As mentioned before, the DATA LED should light up when the RESET button is pressed, and go out when released. This is an indication that the reset circuitry is working correctly. WAIT (24) should be high. BUSREQ (25) high. INT (16) high. A13 (3) bobbing after reset means that the CPU is trying to send information to the printer. NMI (17) high, goes low when TEST pressed.

QUINELLA TEST... What would happen if you had a short between Address 7 and Data bit 3, or A13 and ground, or etc., etc., I don't know, but I dare say the beast won't work at all. How do you find these shorts?? Do what I call a quinella test. Using your meter, check for zero ohms between pin 1 and pin 2 of the Z80. Then check pin 1 and 3, 1 and 4, right up to pin 1 and 40. Step on to pin 2 and 3, 2 and 4 etc., up to pin 2 and 40. Get the idea? You end up checking pin 39 and 40.

Zero ohms will be found at some points, as these points are tied together. Check the circuit to verify these shorts. If a short is found where it shouldn't be, you have found your problem, well at least you know which tracks to look at. This quinella test can be done on all chips if no fault is found at the Z80. Most solder shorts are found at the Dram sockets. Do a quinella test on any socket. Try the 8255 next.

If your printout is almost correct, but you get things like upper case "A" changing to "B" and "1" changing "2" You have data bit zero set all the time. "A" is 41Hex, and "B" is 42Hex, so data bit zero is never clear. You will need an ASCII to Hex lookup table to sort this one out. If you don't understand the Hex jumbo, ASK someone who does. Once you have determined which data bit(s) is faulty, try swapping the chip in this ram position with another to see if the fault conditions change. This will prove the ram chip. In most cases it will not be the ram chip, but your soldering or a faulty socket at the "BAD" location.

I could write a hundred pages and still not cover your problem, but with the above information and a little common sense, you should be able to overcome all but the really obscure fault.

The most common fault found on PBUFF's are User shorted tracks on the solder side of the board at or near the Dram sockets. A quinella test will show these up. The next most common fault for some reason, is a faulty 8255. The EPROM is usually the only item beyond your control. I will always help you out here, but the EPROM is hardly ever the fault.

Provided the buffer is able to operate the printer, if the EPROM data doesn't agree to the built in checksum, A ROM Checksum error is reported to the printer. If no such error is reported, the EPROM is correct.

You will generally know when you have plugged an EPROM in back the front. That is about the only way you can easily damage them. Let me give you a "For Instance". My mate Mick treats EPROMS like you would treat some loose change, just throws them into his shirt pocket and forgets them until he finds them, loses them, or needs them. I go to a bit more trouble than that. But one day Mick trapped me out when he passed two EPROMs onto me and I didn't have a suitable container for them. I put them carefully into my top pocket, my wife washed them in the automatic washing machine, found them, I straightened the legs, read the data that I needed, and then re-programmed them. They might be in your Printer Buffer now...

A SHORT CHAT ON CENTRONICS SIGNALS.... So called Centronics compatible interface signals aren't always compatible. WIRES 1-11 should be the same on most computers/printers, however the Microbee for instance, needs the input

strobe (wire 1) pulse stretched. This is covered in the Microbee engineering notes.

WIRE 12 is the Paper out signal. A high on 12 signals the computer that the printer is out of paper. (PRINTER OUTPUT SIGNAL.)

WIRE 13 is the SLCT (printer selected) A high indicates that the printer is ready to receive data. (PRINTER OUTPUT SIGNAL.) The following lists the major differences of most common types of printers available today. Check your manual for more information.

Wire 14 may be an AUTO-LINEFEED signal. A low on this line will print a line feed after every carriage return. This may be a dip switch setting in the printer. (PRINTER INPUT SIGNAL.)

WIRE 31 may be PRINTER INIT. Low to re-init the printer. (PRINTER INPUT.)

WIRE 32 may be ERROR. Low when paper out, off line, or error. (PRINTER OUTPUT.)

WIRE 36 SELECT IN may need to be low. Could be a dip switch setting in the printer. (PRINTER INPUT SIGNAL.)

WIRES 12, 13 and 32 seem to be the main culprits. The idea is to have your computer handshake with the buffer, and the buffer handshake with your printer.

People are finding new uses for PBUFF all the time. After all, it is a data acquisition and retrieval system. Interfacing to some odd devices has caused headaches. The output busy seems to be one of the problem areas. One user had to double buffer (using two inverters) the O/P busy before it would drive his cash register that has a 390 ohm pull-up resistor.

VERSIONS AND DIFFERENCES.....

V0.0 NOV-84 FIRST SOFTWARE TEST.

V1.0 FEB-85 BASIC 8-64K BUFFER. NO SPECIAL FEATURES.

V1.0 MAY-85 SMALL QUANTITY FOR ROD IRVING ELECTRONICS WITH R.I.E. SIGN-ON NO LONGER SUPPORTED. (SAME AS ABOVE.)

V2.0 SEP-85 SINGLE/MULTIPLE COPY, HEX O/P, BETTER DIAGS.

V3.0 SEP-85 256K VERSION OF ABOVE.

V2.1 OCT-85 SERIAL BUFFER FULL SIGNAL, 32 BYTES BEFORE PBUFF IS FULL. USED CPU A12 AS O/P SIGNAL. (NOT LONGER SUPPORTED)

V3.1 OCT-85 256K VERSION OF ABOVE.

V2.2 JAN-86 DOUBLE BACKSLASH SOFTWARE PAUSE ADDED. " \ " (NO LONGER SUPPORTED.)

V3.2 JAN-86 256K VERSION OF ABOVE.

V4.0 APR-88 DESIGNED MAINLY FOR C3P1 AND FPIO ADD-ON BOARDS BUT DOESN'T OFFER A GREAT DEAL FOR STAND ALONE BUFFER. IMPROVED DIAGNOSTICS AND TRUE HEX DUMP MODE. 1 Mb DRIVERS INCLUDED.

V4.1 JAN-90 SUPPORTS 128K, 512K, AND INCLUDES BOTH 2 AND 4 Mb DRIVERS. (2Mb & 4Mb SIZES STILL TO BE TESTED.)

V4.2 15-MAY-90 DEBUGGED AND TESTED 2 MEG DRIVERS. NOW SUPPORTS 1 MEG OF DRAMS AND 1 MEG MODULE WITH USER WIRED 74LS139.

V4.3 30-MAY-90 REVISED MAIN PROGRAM LOOP IN ORDER TO SPEEDUP GENERAL BUFFERED THROUGHPUT.

V5.0 1-June-92 Verified 4Mb R/W drivers operating correctly. Sign On updated for 4Mb installation. (V4.3 works OK with 4Mb SIMM/SIPP)

V5.1E 4-Aug-93 Assembled to comply with ZLOAD. An "S" Version for Static Ram at 8000H and an "E" Version for EPROM at Zero.

BOARD REVISIONS.....

DEC-84 FIVE PROTOTYPES FOR FIELD TESTING.

REV A. FEB-85 FIRST 8-64K PRODUCTION BOARDS DESIGNED TO FIT STANDARD CASE.

REV B. JUN-85 PIN 1 ALL RAMS JOINED TOGETHER TO ALLOW FOR POSSIBLE EXPANSION TO 256K IF THE SOFTWARE REFRESH OF 41256'S CAN BE ACHIEVED. MINOR CAPACITOR TRACK FAULT CORRECTED. C5 ADDED.

REV C. JAN-86 SERIAL BOARD CONNECTOR ADDED. CLOCK CIRCUIT CHANGED TO TRANSISTOR DRIVER. NEW TEST SWITCH CIRCUITRY ADDED.

REV D. MAR-86 28 PIN EPROM SOCKET PROVIDED. R10 ADDED.

REV E. MAY-86 OPTIONAL HARDWARE PAUSE PADS ADDED. R11 AND "X" PADS ADDED TO ALLOW EASY SELECTION OF 2 VERSIONS OF SOFTWARE IN ONE EPROM.

REV F. MAY-87

NEW DESIGN DOUBLE SIDED BOARD WITH MANY ADDITIONAL FEATURES AS FOLLOWS: A 28 pin socket has been added for future software expansion. (8K static ram, 6264) J3 has been added so that standard 26 pin crimp IDC headers can be used for board interconnections. A double row 26 pin male header can be soldered into this position. J1 & J2 have been retained for existing compatibility with optional boards. J4 (Control) has been set out in a 16 pin dual row header. A header, crimp connector, and 16 wire flat ribbon cable may be used for front panel wiring. R11 was used for high/low ROM selection. R11 is now a pull-up resistor (still 4K7) for the centronics input busy line.

REV G. OCT-87

J1 is now the Z80 bus extended, old J1 & J2 removed, other connector numbers adjusted, 555 timer (E15) C7 and C8 added to produce interrupt driven refresh software, resistor network replaces a lot of 4K7 resistors resulting in resistor ID changes. R6, R7 and R8 added to support 555 timer.

REV H. FEB-89

Provision for 1 Mb dynamic rams using 20 pin sockets and jumper configuration blocks. Diode bridge used instead of discrete diodes. Power LED added. J5 8255 chip select block added for FPIO use. Data bits 6 and 7 swapped to EPROM. (It is now a standard pinout)

REV J. JAN-90

Provision for 64K/256K/1Mb/4Mb Memory Modules (SIMM/SIPP) type using additional 30 pin socket.

REV K. JUN-92

Joined together the artwork of my main PBUFF board and BPIO board in order to save on cable and header costs and generally simplify construction and mounting. Reduced memory configuration links. J7, J8, J9, R10, and R11 added due to the new artwork that adds the old Back Panel I/O board. DB25F and CENT36F now soldered to the main board. Ex, Ey, and Ez User prototype socket positions added. +5V and ground connected to these additional chips. All Configuration links removed on artwork. I found that it is easier for users to add links or jumpers rather than cut tracks. J5 8255 link position moved to allow more room for memory module.

Any constructive comments or criticism on these instructions would be appreciated.

HAPPY COMPUTING DON

** PBUFF Version 3.2 ** by Don MCKENZIE. Jan 86 (C)
29 Ellesmere Cres., Tullamarine AUSTRALIA. 3043
Phone (03) 338 6286

(TEST MESSAGE PRINTOUT.)

256K RAM INSTALLED

OPERATOR INSTRUCTIONS..... (Versions 2.2 and 3.2)

Any time the PBUFF is powered up, with COPY OFF, it is ready to accept data from the computer system. Set to COPY OFF, power up and press TEST. A sign on message complete with buffer memory size is printed. If there is a ROM checksum error, this will be reported on the printout.

Pressing the RESET with COPY OFF will light up the DATA LED very brightly. Release the RESET and the LED will go out. Pressing RESET will abort any current printout, clear the buffer, and set to ASCII (normal) output mode. PBUFF does a RESET on power up.

To use the PBUFF, print your file in the normal manner as per the computer system's operating instructions. The DATA LED will flash as data is accepted by PBUFF, and the printer will start operating. If the file to print is smaller than the PBUFF memory size then the PBUFF will get all DATA from the

computer system, release the computer system for normal operation, and finish the printing job under its own control. If the file to print is larger than the PBUFF memory size then the DATA LED will light up brightly until 256 bytes (100hex.) are free, then PBUFF accepts another 256 bytes from the computer system. This pause can be seen on the DATA LED. When all data is finally loaded into the PBUFF, the LED will stay off and the computer system will be released for normal operation.

COPY.... PBUFF will only copy a file that is the same size or less than the total memory size of the buffer. EG:- A 64K buffer will only allow you to copy a 64K file or less, a 256K buffer will only allow you to copy a 256K file or less. In reality, a 64K buffer will store 65,280 bytes before a buffer overflow occurs and a 256K buffer will store 261,120 bytes. The start of the file to be copied is from the point data was loaded from the last RESET, or power up.

If the TEST function was used after power up, this printout will be stored at the start of the buffer to be copied. A RESET can be used to clear this data from the buffer to be copied. To copy a file, set PBUFF to COPY OFF, press reset, load the file into PBUFF, and allow it to print. When finished, throw the copy switch to ON, then to OFF. An exact copy of the printed file will be produced. If multiple copies are required, leave the copy switch in the ON position. This will print the same file over and over until your printer runs out of paper, RESET is pressed, or COPY is set OFF.

COPY ON Test function... Press RESET, set to COPY ON, press RESET. The LED will flash at approx. 3 cycles per second. This indicates a pass of system diagnostics. If at any time the LED flashes at approx. 1 CPS. then you have a RAM error. Setting COPY OFF will stop this test and ready the buffer.

Hexadecimal Output... Press RESET, set COPY ON, press TEST. LED will flash at approx. 3 CPS. Set to COPY OFF. PBUFF will now output all data in HEX format as follows :- MSB, LSB, space. As this requires three times the memory overhead to store, you can divide your buffer size by three. To abort printout or set back to ASCII (normal) mode, press RESET. BEWARE of internal printer buffer confusion in the HEX mode. As all output including control characters are converted to printable characters, the internal printer buffer is never "FORCED" to empty its contents. A known dummy file may need to be loaded into PBUFF in order to "FORCE PRINT" any remaining characters in the original file. Setting COPY ON then OFF will print the same file again, which will also "FORCE PRINT" the remaining characters.

HARDWARE PAUSE SWITCH (IF FITTED.)..... Setting pause on (switch contacts open) will stop all output to the printer. Input will continue as normal. Setting pause off allows the printer to continue. Can be used in conjunction with the printer sharer switch as follows:- During printout, select pause, swap printers then release pause. No characters will be lost, and no "lock-up" conditions will occur.

** PBUFF Version 5.1E ** by Don McKENZIE. Updated August 4, 1993(c)
29 Ellesmere Cres., Tullamarine AUSTRALIA. 3043

Phone (03) 338 6286

Available memory sizes are:-

(01) 64K, (02) 128K, (04) 256K, (05) 320K, (08) 512K,
(16) 1024K, (17) 1088K, (20) 1280K, (32) 2048K, and (64) 4096K
(xx) = Number of possible 64K pages available.

0123456789

ABCDEFGHIJKLMNPOQRSTUVWXYZ

(TEST MESSAGE PRINTOUT.)

abcdefghijklmnopqrstuvwxyz

4096 K BYTES RAM INSTALLED (64 Page(s) by 65,536 bytes.)

OPERATOR INSTRUCTIONS..... (Version 5.1E)

Any time the PBUFF is powered up, with COPY OFF, it is ready to accept data from the computer system. Set to COPY OFF, power up and press TEST. A sign on message complete with buffer memory size is printed. If there is a ROM checksum error, this will be reported on the printout.

Pressing the RESET with COPY OFF will light up the DATA LED very brightly. Release the RESET and the LED will go out. Pressing RESET will abort any current printout, clear the buffer, and set to ASCII (normal) output mode. PBUFF does a RESET on power up.

To use the PBUFF, print your file in the normal manner as per the computer system's operating instructions. The DATA LED will flash as data is accepted by PBUFF, and the printer will start operating. If the file to print is smaller than the PBUFF memory size then the PBUFF will get all DATA from the computer system, release the computer system for normal operation, and finish the printing job under its own control. If the file to print is larger than the PBUFF memory size then the DATA LED will light up brightly until 256 bytes (100hex.) are free, then PBUFF accepts another 256 bytes from the computer system. This pause can be seen on the DATA LED. When all data is finally loaded into the PBUFF, the LED will stay off and the computer system will be released for normal operation.

COPY.... PBUFF will only copy a file that is the same size or less than the total memory size of the buffer. EG:- A 64K buffer will only allow you to copy a 64K file or less, a 256K buffer will only allow you to copy a 256K file or less. In reality, a 64K buffer will store 65,536 bytes before a buffer overflow occurs and a 256K buffer will store 261,141 bytes. The start of the file to be copied is from the point data was loaded from the last RESET, or power up. To copy a file, set PBUFF to COPY OFF, press reset, load the file into PBUFF, and allow it to print. When finished, throw the copy switch to ON, then to OFF. An exact copy of the printed file will be produced. If multiple copies are required, leave the copy switch in the ON position. This will print the same file over and over until your printer runs out of paper, RESET is pressed, or COPY is set OFF. COPY ON Test function... Press RESET, set to COPY ON, press RESET. The LED will flash at approx. 4 cycles per second. This indicates a pass of system diagnostics. Setting COPY OFF will stop this test and ready the buffer.

Hexadecimal Output... Press RESET, set COPY ON, press TEST. LED will flash at approx. 4 CPS. Set to COPY OFF. A carriage return and line feed will be

stored first in the buffer. PBUFF will now output the next file in a HEX dump format. This complies to a normal utility type format of ADDRESS, HEX data, and ASCII data in three separate columns. This expansion requires about four times the memory overhead to store. The address is only a byte count unless you dump a machine language program in which case it may have some relevance. To abort printout press RESET. Any characters outside the normal ASCII set are converted to a period "." in the ASCII column. If incoming data is not detected within eight seconds then end of file is assumed and PBUFF builds the last block of the dump complete with a last byte count and sets back to the ASCII (normal) mode. All characters after the last byte are printed as a NULL or zero byte.

HARDWARE PAUSE SWITCH (IF FITTED.)..... Setting pause on (switch contacts open) will stop all output to the printer. Input will continue as normal. Setting pause off allows the printer to continue. Can be used in conjunction with the printer sharer switch as follows:- During printout, select pause, swap printers then release pause. No characters will be lost, and no "lock-up" conditions will occur.

PBUFF PROBLEMS AND FIXES.... UPDATED August 4, 1993

Some of this information dates back a while now, but I do need to keep adding to it. The oldest info is pushed down. Sounds like a stack.

FPIO..... (Front Panel I/O)

Don't build up a PBUFF and FPIO together. Get the PBUFF going first, test it, then install the FPIO. Many kit builders have come unstuck by trying to get two unknown chunks of hardware going together. Simplify it by building and testing one item at a time. I call this SECTION ISOLATION.

RESISTOR R11 was 1K. I have changed this to 270 Ohms. This resistor is used to pull the paper empty signal low. My latest IBM Notebook (1993 Model) detected this signal as being high. It must have a very low value pull-up resistor inside that couldn't pull this signal low. The PE signal can be grounded at PBUFF as this input to the computer is an open collector signal, but for safety reasons, I decided to pull it low via a resistor.

PBUFF DRAM PINOUT CONFUSION....

A 20 pin socket is used for the DIP version Drams. The pinout must first be related to either a 16 or 18 pin socket depending on Dram type. When the true pinout is determined from the overlay taking into account the pin 1 position and memory links, this can then be checked against a data sheet. All pins except the address pins should line up with the data sheets. I have had to shuffle the address lines to match up with all memory sizes and organize the address lines that require software refresh. All 16 and 18 pin Drams tried to date have worked with PBUFF.

AMIGA COMPUTERS....

Some early model AMIGA's have experienced problems sending data to PBUFF. Two independent fixes have been sent to me and user feedback tells me that these fixes do overcome the problem. Fix (1) should do the job on its own. These two fixes are as follows:-

(1) At the AMIGA end link BUSY and NOT ACK. Disconnect NOT ACK to the BPIO board.

(2) Install a faster crystal to PBUFF. If a 6Mhz crystal is fitted, you may need a Z80B before PBUFF will run. (Don't forget 330 ohm pullup)

TANDY PRINTERS....

A Tandy technician swears that most Tandy printers have been designed not to work with standard Centronics signals, for reasons that only Tandy know. This is a common trick of Tandys with peripherals. He states that if you disconnect pin 33 to the printer it will work with PBUFF.

C3P1 BOARD.... (Computers 3 Printer 1)

J6 pins 1 and 2 are not used with the current software however the status of this spare link can be read with user written software.

COMMODORE C64 AND MY SERIAL BOARD....

I have been asked the question so many times that I decided to save myself a lot of trouble by creating this file. I have sold several serial boards to COMMODORE 64 users with the view to interfacing the two. As yet, not one person has given me any feedback, so I can't guarantee the results. I designed the serial board with provision for TTL inputs. This was done to match the C64 port.

TANDY COLOR COMPUTERS....

The first computer tested with my serial board was the Tandy COCO. Pin connections are shown in the assembly instructions.

SERIAL BOARD DOUBLE CHARACTERS....

One user had a PBUFF connected to a serial board fed as an input to COM 1 of a PC type machine for a dedicated application. He found that each character was transmitted twice. To overcome this, he connected a third diode from pin 24 of the UART (anode end) to the existing "ORED" junction of D4 and D5.

DOUBLE THE MEMORY CAPACITY OF YOUR PBUFF PRINTER BUFFER....

(2Mb maximum available using 1Mb chips.)

My PBUFF printer buffer (Rev. K) memory capacity can now be very easily expanded. This has been possible with PBUFF Version 4.2 and later versions.

Version 5.0 and upwards is now the current default supplied software and has been supplied since June 1, 1992.

Adding a simple one chip 74LS139 decoder circuit, memory capacity is now capable of being doubled using additional standard 64K, 256K or 1Mb by 1 bit dynamic rams (DRAMs) or 8 and 9 byte wide SIPP/SIMM 64K, 256K, or 1Mb type memory modules. The extra byte is ignored by PBUFF. Please note that this arrangement will require approximately 230 ma more in the power supply department so I would recommend that a 600 ma to 1 amp plugpack or transformer be used.

The older, and not to be confused version 3.2/2.2 EPROM is still available. This supports 8K, 16K, 32K, and 64K using 1, 2, 4, or 8 by 4164's, and 256K

using 8 by 41256's. This version doesn't need the 6264 static ram or 555 timer installed, and in fact will not work with the timer installed.

The Memory sizes available with Version 5.1E PBUFF are:-

1	page	64K	8 by	64K DIP or 1 by 64K SIMM.
2	pages	128K	16 by	64K DIP (piggy-back) or 8 by 64K DIP & 1 64K SIMM
4	pages	256K	8 by	256K DIP or 1 by 256K SIMM.
5	pages	320K	8 by	256K DIP and 1 by 64K SIMM.
8	pages	512K	16 by	256K DIP (piggy-back) or 8 by 256K DIP & 1 256K SIMM
16	pages	1024K	8 by	1024K DIP or 1 by 1024K SIMM.
17	pages	1088K	8 by	1024K DIP and 1 by 64K SIMM.
20	pages	1280K	8 by	1024K DIP and 1 by 256K SIMM.
32	pages	2048K	8 by	1024K DIP and 1 by 1024K SIMM.

64 pages 4096K 1 by 4096K SIMM only. Larger sizes not yet available.

The sizes up to 2Mb can also be organized by swapping the order of combinations of DIP type Drams and SIPP/SIMM type modules. This is explained in more detail later on.

HOW TO PIGGY-BACK MEMORY CHIPS.... (if required for 128K and 512K) After the following surgery you should have eight DRAM chips, each one with another DRAM soldered on top of it. Get a vice and clamp an old socket into it facing up. If you have a TANDY IC Pin Aligner tool, (276-1594 @ \$5.95 and a great little device!) you can use this to straighten the legs of the sixteen DRAMs you have selected to piggy-back. These must all be of the same type, all 4164s, or all 41256s.

All pins except one are parallel wired between two memory chips. This one pin exception is the column address strobe pin. (CAS*) I will now give you this pin number. This is very IMPORTANT. This pin number is referenced to the DRAM pinout, not the circuit, as the circuit pinout refers to a 20 pin socket not a memory I.C. pinout. The CAS* pin is pin 15. Install one DRAM firmly into the old socket. On a second DRAM bend the CAS* pin out at right angles. Place the second DRAM on top of the socketed DRAM so that all pins except the CAS* pins are just touching each other. Solder two opposite corner pins together and check and adjust for physical parallel alignment. When you are satisfied, solder all other touching connections. The lower CAS* pin should be in the socket. The upper CAS* pin should be sitting out at right angles to all other pins and all other pins should be parallel connected.

With a sharp pair of sidecutters snip the upper CAS* pin off so that just a small pad remains. Tin this pad now so that you can solder a wiring connection to it later on. Remove the new stacked memory chip from the socket and place it aside. Repeat this procedure another seven times to create a total of eight individual units. All of the upper CAS* pads must now be connected together using insulated wire.

The easiest way of doing this is to insert these 8 units into your PBUFF board memory sockets. Observe the normal installation procedure for installing these DRAMs regarding the M1 to M7 memory configuration links. The upper CAS* signals can now be wired together. Include a short floating tail on one end of this daisy chained connection. The floating wire will be

used for the new memory decode. This is now given the new signal name of CAS1*. The lower CAS* signal is now CAS0*.

DIP DRAM INSTALLATION.... Install a set of eight by DRAMs into the memory sockets observing the DRAM type installation procedures given in the manual. The CAS* of these DRAMs will now become CAS0*.

MEMORY MODULE INSTALLATION.... Install A memory module into the 30 pin socket. Cut the track going to the CAS* pin (pin 2) of the memory module and solder a short insulated wire to this pin. This signal is now CAS1*.

ALTERING THE MEMORY MODULE SOCKET.... The printed circuit board tracks pick up several signals from the DRAM sockets for the memory module. If you are installing 64K or 256K chips into the sockets then the memory module connections are correct, but if you are installing 1Mb or larger DRAMs into the sockets then three signals have to be altered to the memory module. Cut the tracks going to pins 4, 5 and 7 of the memory module. Connect pin 4 of the memory module to the Z80 pin 36 (A6). Connect pin 5 of the memory module to the Z80 pin 33 (A3). Connect pin 7 of the memory module to the Z80 pin 30 (A0).

INITIAL TESTING OF THE NEW DOUBLE MEMORY.... Both banks of memory can now be tested on an individual basis to prove your soldering and test all memory chips.

One user installed Link needs to be removed at the M1 jumper block so that CAS* from the 74LS00 can be isolated from the CAS0* signal. This new CAS0* signal is the normal CAS* pin of the socketed DRAMs. A look at Figure 1 will show the M1 block in detail viewed from the component side of the board. The wiring posts are laid out in the same order as the board itself. Whichever way you went about installing the CAS link across the M1 block, you must now remove this link so as to isolate CAS from CAS0.

Figure 1 is drawn with no jumpers installed to save confusion. Use a 1K to 10K resistor to pull CAS1* high to +5 volts by soldering this resistor between +5 volts and the CAS1* insulated wire tail. This will disable the second bank of memory. Connect CAS* to CAS0*.

The buffer can now be tested at the single level memory size. Now disconnect both CAS0* and CAS1* and swap them so that CAS0* connects to the resistor and CAS1* connects to CAS*. You can again test your buffer to prove your second bank of memory at the single level capacity. The PBUFF test message will tell you how much memory you have installed.

MEMORY DOUBLER CIRCUIT.... Figure 1 gives details of wiring up the added 74LS139 memory decoder used to synchronize the CAS* signals which perform the memory doubling. Point AX input must be wired to the appropriate Z80 address line to suit the memory size. For 128K wire AX to pin 1 (A11) of the Z80. For 320K and 512K wire AX to pin 38 (A8) of the Z80 and for 1088K, 1280K, and 2 Mb wire it to pin 39 (A9) of the Z80. This additional chip may be mounted in socket position Ex. The ground and +5Volts are already connected to Ex.

FULL MEMORY TESTING.... Once the doubler circuit is wired up correctly, a

test message printout of the buffer will prove the results. The software auto-configures its read and write routines to your new memory size. If for any reason you wish to remove your second bank of memory, the input CAS* must be re-connected to the socketed DRAM CAS* which is back to the original circuit, and the CAS0* signal must be removed. And that is all there is to it.

SWAPPING THE MEMORY SIZE COMBINATIONS.... I have given a list of the number of 64K pages available for Ver 5.1E PBUFF. This gives a combination of DIP, SIMM type installations. These installation combinations can be reverse installed if required. All you have to do is swap the CAS0* and CAS1* connections so that CAS0* always connects to the largest memory size installation. If the memory sizes are equal, the circuit will work either way. The normal installation procedures for DIP and SIMM combinations are given in this article.

4Mb (18 PIN) DRAM INSTALLATION.....

The 4Mb BUFFER is mentioned in the main assembly instructions. To date, I haven't seen 4Mb DRAMs in a DIP package, however the SIMM/SIPP types are now readily available. I have left the instructions regarding 4Mb DIPs intact just in case they appear in future.

The standard 4 Mb DRAMs will use pin 5 of the socket (pin 4 of the DRAM) as the added address line. This signal must be isolated at the M1 header block and jumpered to pin 39 (A9) of the Z80. All other signals are pin for pin compatible with the 1 Mb DRAMs so the other M1 to M7 blocks must be hooked up for 1 Mb operation. The DRAMs must be installed to match the 1 Mb socket installation.

EPROM AND BOARD UPDATES....

Version 5.1E EPROM is available for \$20. This price includes postage, full instructions on disk, (as described earlier) and royalty.

Please note **** Ver 5.1E is only readily suitable for board revisions that have provision for the 555 timer and 6264.

Pre Rev. H boards will need to have data bits 6 and 7 swapped to the EPROM socket. Two small pads right next to pins 18 and 19 under the EPROM socket on the solder side of the board can be used to isolate and cross these connections. This swap was done in attempt to discourage piracy using the hardware method, but as I have found out, It was more trouble than it was worth.

I believe that if I can put out a double sided plated through board kit at the right price, who would be really want to hardwire it? The current (now Rev. K) PBUFF board is available on its own for \$35, yes you can use it for any project you like!.
